PVP 19

Code: 19EC3302,19EE3302

II B.Tech - I Semester – Regular Examinations – MARCH 2021

ELECTRONIC DEVICES AND AMPLIFIER CIRCUITS

(Common for ECE, EEE)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 5 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each question carries 12 marks.
4. All parts of Question paper must be answered in one place

PART – A

1. a) Draw the small signal models of *npn* and *pnp* transistors.
   b) Consider a process technology for which L_{min} = 0.4μm, t_{ox} = 8nm, μ_n = 450 $cm^2/V \cdot s$, and V_t = 0.7V. Find C_{ox} and k'_n assume the values of other parameters, if required.
   c) Compare MOSFET and BJT devices.
   d) Discuss the operation of MOS differential pair.
   e) Explain the operation of CMOS OpAmp.

PART – B

UNIT – I

2. a) Draw the basic construction and equivalent circuit of a Bipolar Junction Transistor. Briefly explain the base width modulation. 6 M
   b) A transistor for which $I_s = 10^{-16}$ A and β = 100 is conducting a collector current of 1 mA. Find υ_{BE}. Also, find I_{SE} and I_{SB} for this transistor. 6 M

OR

3. a) Explain the working of CE and CB amplifiers. 6 M

b) Consider a *pnp* transistor with υ_{EB} = 0.7 V at i_E = 1 mA. Let the base be grounded, the emitter be fed by a 2-mA constant-current source, and the collector be connected to a –5-V supply through a 1- kΩ resistance. If the temperature increases by 30°C, find the changes in emitter and collector voltages. Neglect the effect of I_{CBO}. 6 M

UNIT – II

4. a) Discuss biasing in MOS amplifier circuits in common source configuration. 6 M

b) Compare the enhancement mode and depletion mode MOS transistors. 6 M

OR

5. a) Explain common gate and common drain amplifiers in detail. 6 M

b) A CG amplifier is required to match a signal source with R_{sig} = 100Ω. At what current I_D should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 kΩ, what overall voltage gain is realized? 6 M

UNIT-III

6. a) Explain the working of Wilson current mirror. 6 M

b) For β = 100 and r_0 = 100 kΩ, contrast the Wilson mirror and the simple mirror by evaluating the transfer-ratio error due to finite β, and the output resistance. 6 M

OR

7. a) For a cascode MOS mirror utilizing devices with V_t = 0.5 V, $\mu_n C_{ox}$ = 387 μA/V^2, V'_A = 5 V/μm, W/L = 3.6 μm, and I_{REF} = 100 μA, find the minimum voltage required at the output and the output resistance. 6 M

b) Explain the operation of cascode current mirror. 6 M

UNIT – IV

8. a) Discuss the importance of stability factor in amplifier design. 6 M

b) Discuss about low and high frequency response of common drain amplifiers. 6 M

OR

9. a) Explain small-signal operation of the MOS differential pair. 6 M

b) Explain large signal operation in differential amplifier. 6 M

UNIT – V

10. a) Discuss MOS differential amplifier with active load. 6 M

b) Discuss multistage MOS amplifiers. 6 M

OR

11. a) Explain input offset voltage of MOS differential pair. 6 M

b) Explain input bias and offset currents of MOS pair. 6 M